Patent claims

1. An arrangement applied to a node in a communication network, said node comprising one or more time slot buses transferring frames from a number of serial input lines located on a receiving side of the node to a number of serial output lines located on the transmitting side of the node, the serial input/output lines each having one respective FIFO into/from which bits corresponding to the associated serial line are shifted,
characterized in

one or two data buffers for each time slot bus at the receiving side buffering the frames from the input lines before transmission, the data buffer being shared between all the input lines by means of respective pointers allocating one memory area in the data buffer for each of the input lines,

a scheduler consecutively checking the input lines for data transfer requests, and if a data transfer request exists, transferring one or more data byte(s) associated with the input line corresponding to the data transfer request to the data bus buffer,

a timer for each input line indicating the time at which data transfer requests for the respective input line are to occur.

2. Arrangement according to claim 1,
characterized in that a pointer contains a data bus address of the first bite of the data area it is allocating.

3. Method according to claim 1 or 2,
characterized in that there is one connection table for each time slot bus at the receiving side, each entry in the connection table contains at least

a data bus address pointing to a byte in the associated data buffer, the entries are arranged in the same order as their corresponding bytes are to be transferred on the data bus, and a counter, synchronized to a clock used by the time slot bus for transmission of timeslots, indicates which byte in the associated data buffer that presently is to be read out from the data bus buffer into a time slot in the associated data bus by indexing the entries of the connection table.

4. Arrangement according to any of the preceding claims, c h a r a c t e r i z e d i n that the scheduler is checking the input lines for data transfer requests by using a round-robin scheme on a transfer request register containing one entry for each input line indicating if a data transfer request for the respective input lines exists.

5. Arrangement according to any of the preceding claims, c h a r a c t e r i z e d i n that the time at which data transfer requests for an input line are to occur is dependent on the number of data bits to be transferred from the input line to the data bus buffer during one frame, the number of clock cycles from the header of a frame to the first data transfer request, the average number of clock cycles between each transfer, and the resolution for the average number of clock cycles between each transfer.

6. Arrangement according to any of the preceding claims, c h a r a c t e r i z e d i n that frames may be transmitted through the time slot buses either in a minimum delay modus or in a constant delay modus, in case of minimum delay, bytes from an input line are transferred over a time slot bus in the same order as they arrived the input line, and in the case of constant delay, bytes in transfer on a time slot bus are identifiable and bytes from an input line may be transferred over a time slot bus in an order different from the order they arrived the input line.

7. An arrangement applied to a node in a communication network, said node comprising one or more time slot buses transferring frames from a number of serial input lines located on a receiving side of the node to a number of serial output lines located on the transmitting side of the node, the serial input/output lines each having one respective FIFO into/from which bits corresponding to the associated serial line are shifted,
c h a r a c t e r i z e d i n

one or two data buffers for each time slot bus at the transmitting side buffering the frames from the one or more time slot buses before forwarding to the output line, the data buffers being shared between all the output lines by means of respective pointers allocating one memory area in a connection table for each of the output lines, each entry in the connection table contains at least a data bus address pointing to a byte in one of the data buffers, the entries are arranged in the same order as their corresponding bytes are to be transferred to an output line,

a scheduler consecutively checking the output lines for data transfer requests, and if a data transfer request exists, transferring one or more data byte(s) associated with the output line corresponding to the data transfer request from one of the data bus buffer to that output line,

a timer for each output line indicating the time at which data transfer requests for the respective output line are to occur.

8. Arrangement according to claim 7,
c h a r a c t e r i z e d i n that a pointer contains a connection table address of the first entry in the data area it is allocating.

9. Arrangement according to any of the preceding claims, characterized in that the scheduler is checking the output lines for data transfer requests by using a round-robin scheme on a transfer request register containing one entry for each output line indicating if a data transfer request for the respective output lines exists.

10. Arrangement according to any of the preceding claims, characterized in that the time at which data transfer requests for an output line are to occur is dependent on the number of data bits to be transferred from a data bus buffer to the output line during one frame, the number of clock cycles from a frame start to the first data transfer request, the average number of clock cycles between each transfer, and the resolution for the average number of clock cycles between each transfer.